Compositional Verification of PLC Software using Horn Clauses and Mode Abstraction

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Outline

Introduction

CHC-based Verification

- Constrained Horn Clauses
- Modelling of PLC Software with CHCs
- Mode-Space as Call Summary
- Experiments

Conclusion

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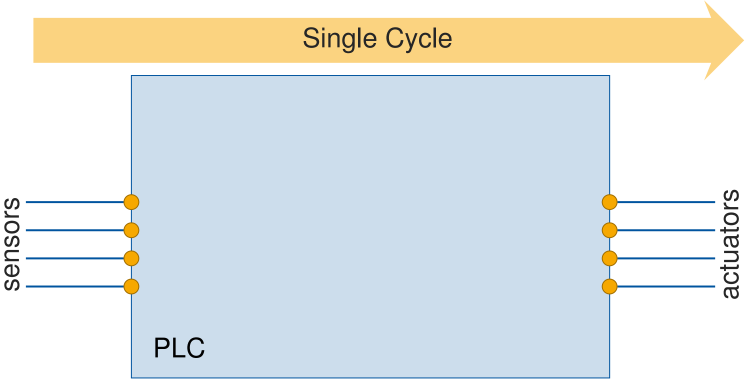
- PLCs are devices tailored to the domain of industrial automation, e.g. for actuating valves of a tank
- Realise reactive systems, repeatedly executing the same task



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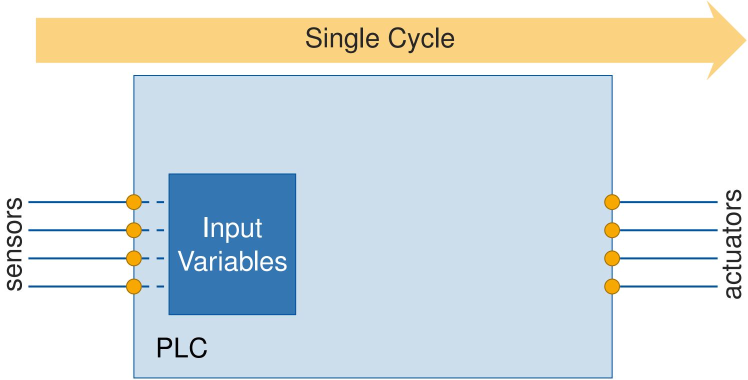

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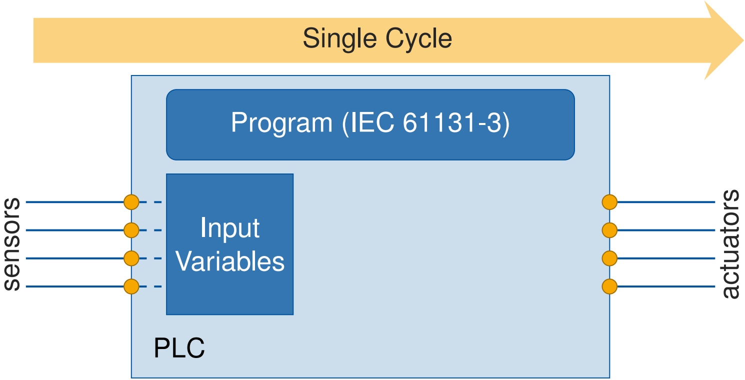

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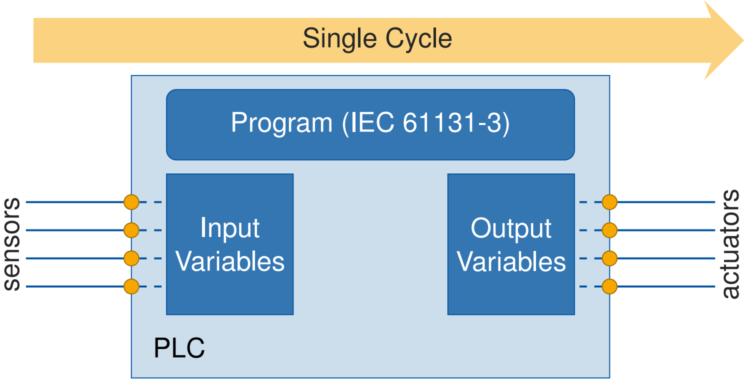

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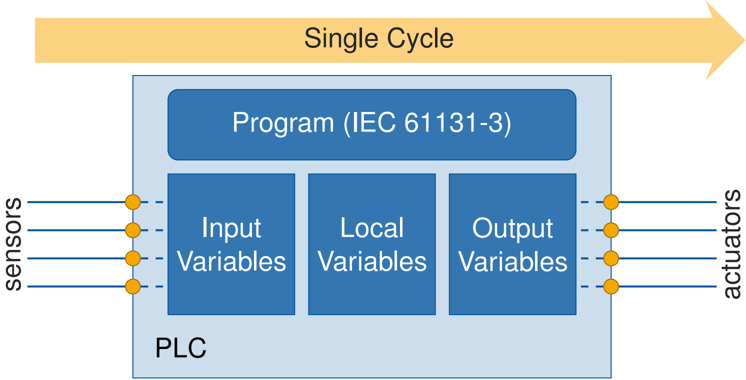

Running Example

- Implements delegation of requests
- Input in forwarded on rising edge for req
- ReqHandler h is polled in every cycle
- Exhibits state-machine semantics via DiagCode

```
PROGRAM Main
  VAR_INPUT  req:BOOL; in:WORD;      END_VAR
  VAR        m  :BOOL; h :ReqHandler;END_VAR
  VAR_OUTPUT out:WORD;               END_VAR
  // Forward data on rising edge
  IF (req AND NOT m) THEN
    h(data:=in, res=>out);
  ELSE
    h(res=>out);
  END_IF
  m:=req;
END_PROGRAM

FUNCTION_BLOCK ReqHandler
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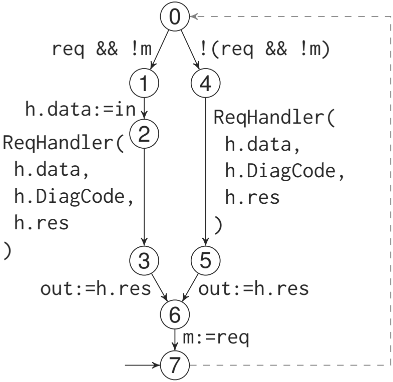

Figure: Main CFA of example

"Idle"
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"Processing"
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"Error"
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Figure: Mode space of ReqHandler

- Requests are processed in $\leq$ two execution cycles?

$\Rightarrow$ On request, "Processing" mode is reached in a single cycle

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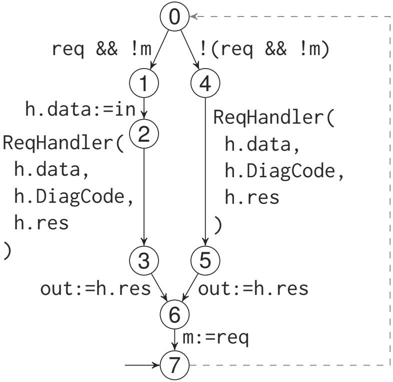

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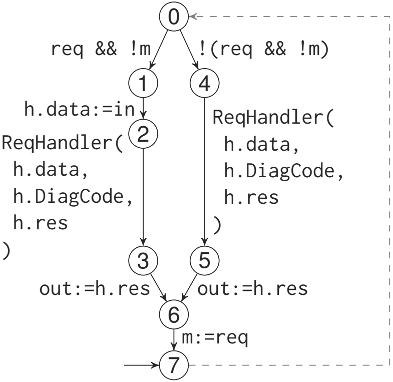

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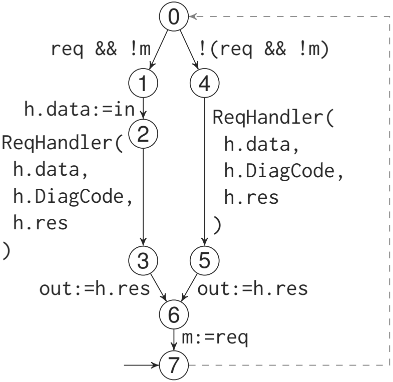

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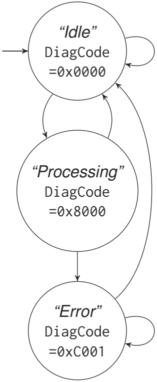

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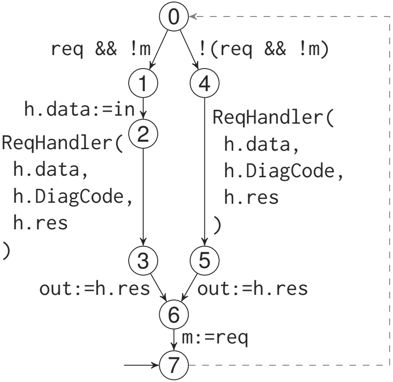

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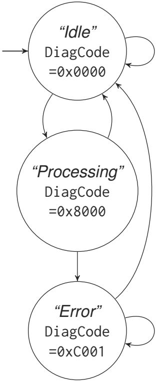

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Requirements Towards Formalism & Model Checker

- Compositional reasoning (no cloning or inlining)
- Integrates with abstraction of calls (call summaries)

Example

- Let `f1:FB; f2:FB;`
- Reason about `FB(...)`
- Avoid `f1(...)`, `f2(...)` and instruction cloning

Example

- Consider $\mathrm{abs}(x) = y$
- Use summary

$$y \geq 0$$

- Until details needed

- Constrained Horn Clauses (CHCs) meet these
- Uniform formalism for symbolic model checking of software

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Constrained Horn Clauses

- Special case of Satisfiability Modulo Theories (SMT)

Definition

Given sets of variables $\mathcal{V}$, function symbols $\mathcal{F}$, and predicates $\mathcal{P}$, a *Constrained Horn Clause* (CHC) is a formula

$$\forall \mathcal{V}\ \underbrace{p_1(\vec{X}_1) \wedge \cdots \wedge p_k(\vec{X}_k) \wedge \varphi}_{\text{body}} \rightarrow \underbrace{h(\vec{X})}_{\text{head}},\ k \geq 0,$$

where

- $\vec{X}_i, \vec{X} \subseteq \mathcal{V}$ are possibly empty vectors of variables
- φ is a constraint over $\mathcal{F}$ and $\mathcal{V}$

- CHCs satisfiable if satisfying interpretation of p_i exists

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Concept

For each block type A with signature $VarTypes$, add a predicate

$$p_A : \underbrace{Loc \times VarTypes}_{source} \times \underbrace{Loc \times VarTypes}_{target} \to \mathbb{B}$$

- Will define transitive reachability within A

⇒ Observable semantics of procedure captured by

$$p_A(\underbrace{l_{entry}}_{const}, \vec{X}, \underbrace{l_{exit}}_{const}, \vec{X}')$$

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Encoding a Transition

Variables instances:

- $\vec{X} = (req, in, m, h.data, h.DiagCode, h.res, out)$
- $\vec{X}' = (req', in', m', h.data', h.DiagCode', h.res', out')$

Transitive Reachability:

$$p_{Main}(l, \vec{X}, 1, \vec{X}')$$
$$\wedge\ h.data'' = in' \wedge id(X' \setminus \{h.data'\})$$
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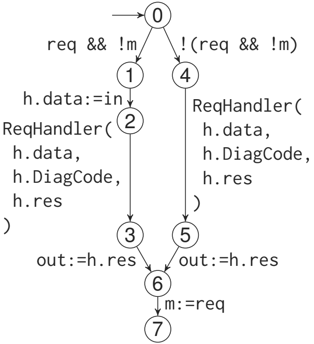

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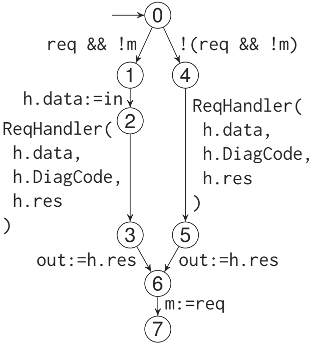

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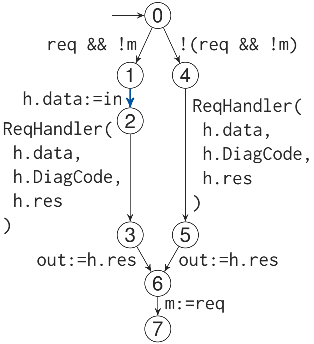

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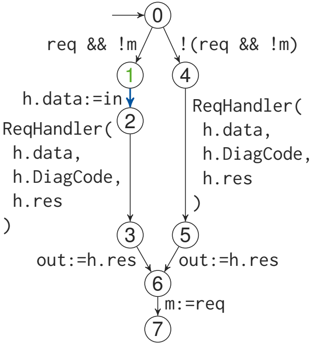

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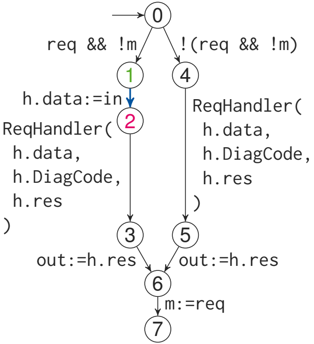

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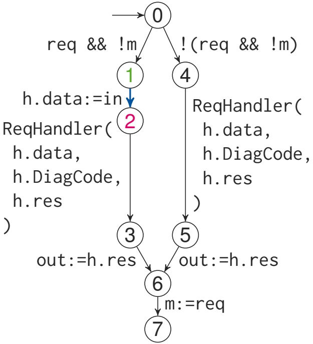

Encoding a Call

Variables instances:

$$\vec{X} = (req, in, m, \underbrace{h.data, h.DiagCode, h.res}_{\vec{X}_h}, out)$$

Transitive Reachability (& call summary):

$$
\begin{aligned}
& p_{Main}(l, \vec{X}, 2, \vec{X}') \\
\wedge\ & p_{ReqHandler}(0, \vec{X}'_h, 42, \vec{X}''_h) \wedge id(\vec{X}' \setminus \vec{X}'_h) \\
\wedge\ & S_{ReqHandler}(\vec{X}'_h, \vec{X}''_h) \\
\rightarrow\ & p_{Main}(l, \vec{X}, 3, \vec{X}'')
\end{aligned}
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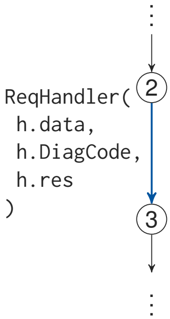

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)
```

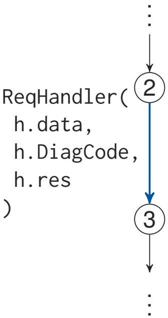
Encoding a Call

Variables instances:

$$\vec{X} = (req, in, m, \underbrace{h.data, h.DiagCode, h.res}_{\vec{X}_h}, out)$$

Transitive Reachability (& call summary):

$$\begin{aligned} & p_{Main}(l, \vec{X}, 2, \vec{X}') \\ \land\ & p_{ReqHandler}(0, \vec{X}'_h, 42, \vec{X}''_h) \land id(\vec{X}' \setminus \vec{X}'_h) \\ \land\ & S_{ReqHandler}(\vec{X}'_h, \vec{X}''_h) \\ \rightarrow\ & p_{Main}(l, \vec{X}, 3, \vec{X}'') \end{aligned}$$



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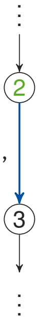

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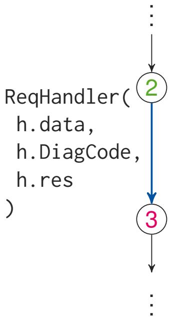

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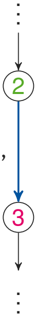

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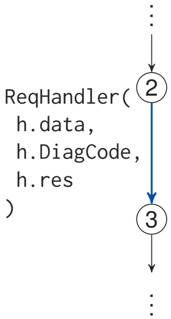

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Checking Safety Specifications

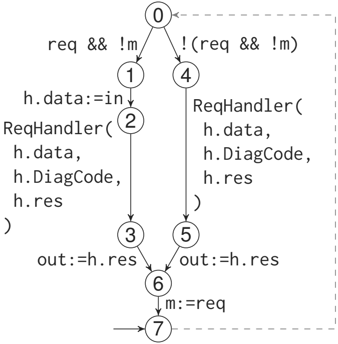
- Does safety property $safe(\vec{X})$ hold at the end of every cycle?

⇒ Yes, if adding

$$p_{Main}(0, \vec{X}, 7, \vec{X}') \rightarrow safe(\vec{X}')$$

keeps CHCs satisfiable

- Violated, if unsatisfiable



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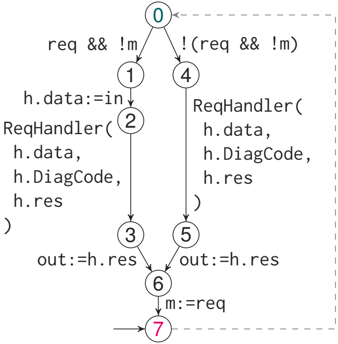

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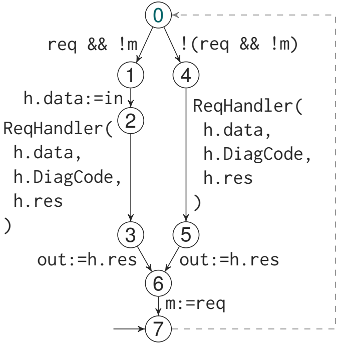

Approximating the Mode-Space

Idea:

- Procedure's complexity needs to be low w.r.t. CHC-solving

⇒ Adapt value-set analysis (VSA) to determine mode-transitions

Procedure:

1. Use global VSA to approximate all variables' values
2. For each function block type, e.g. `ReqHandler`
   2.1 For each computed mode-value, e.g. $\{$`0, 0x8000, 0xC001`$\}$
      - Keep global VSA values but fix mode, e.g. set `DiagCode=0`
      - Compute block's single-cycle VSA
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Mode-Space as Call Summary

- Mode-space constrains possible transitions

⇒ Yields call summary $S_{ReqHandler}(\vec{X}_h, \vec{X}'_h)$:

$$\begin{aligned}
&(h.DiagCode = \mathtt{0} \rightarrow h.DiagCode' = \mathtt{0} \\
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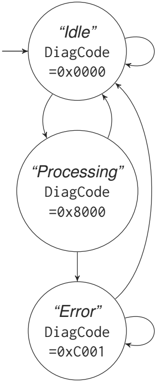

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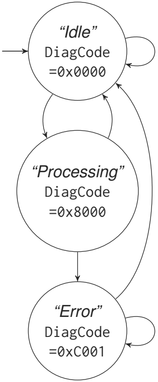

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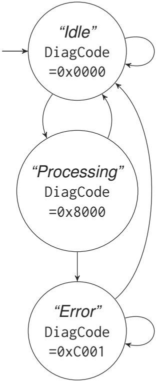

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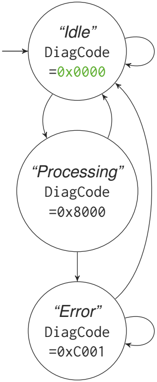

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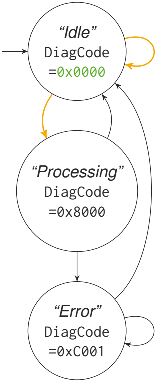

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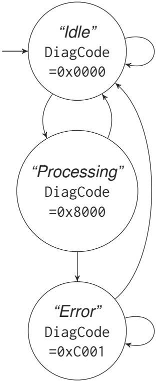

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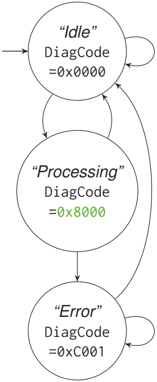

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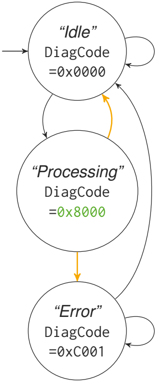

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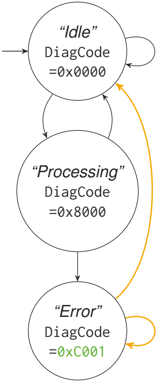

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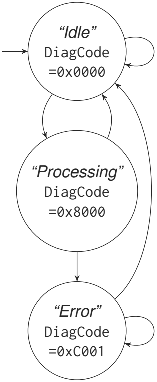

Benchmarks

- Two groups of PLC programs from PLCopen Safety library
  - elementary modules implementing safety concepts (23 specs)
  - user examples composed of elementary ones (17 specs)
- Elementary modules exhibit mode-semantics via `DiagCode`
- We check invariants taken or derived from PLCopen
- CHC-solving via Z3's Property Directed Reachability (PDR)

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Results

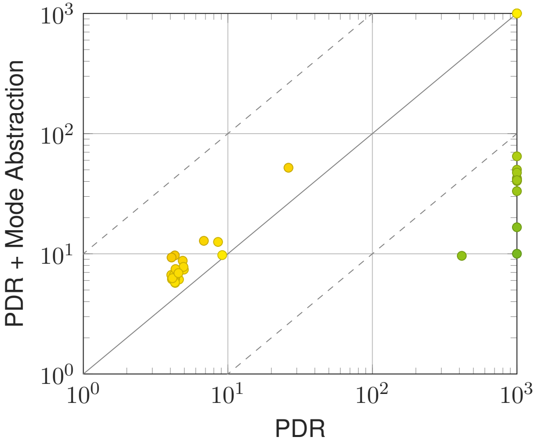

Figure: Time [s] spent on verification of each task

Summary

- Logic control applications exhibit mode-semantics
- Mode-space contains global information
- Approximate mode-abstraction possible via VSA
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  - compositional characterisation and reasoning
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Related Tools & Techniques

Mode-Abstraction:

- Predicate abstraction [GS97]
- Abstract-domain selection based on variable usage [Ape+13]

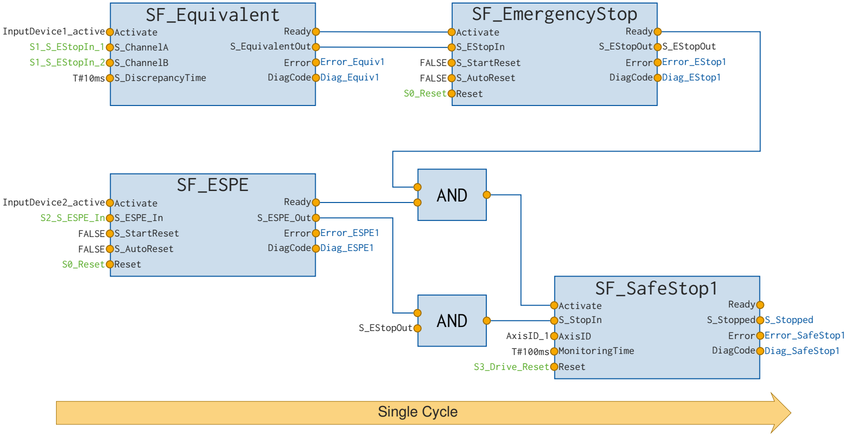
Recent years:

- Decoupling Language Details from Verifier Implementations
- Modular structure & off-the-shelf components

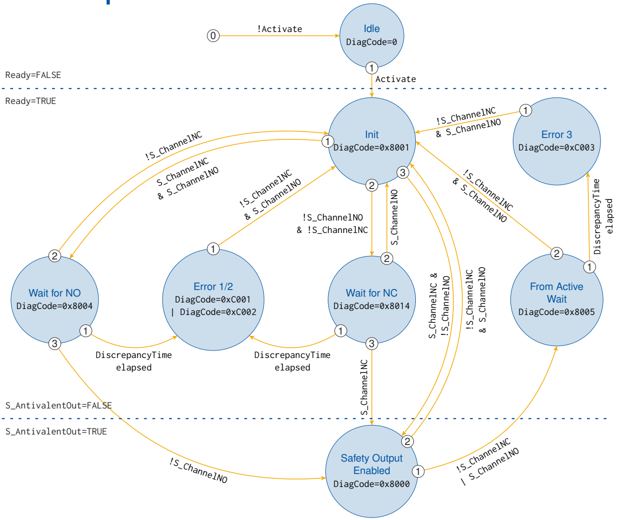
Intermediate Verification Language:

- BOOGIE [Lei08]
  - used by SMACK [RE14]
  - checked by CORRAL [LQL12]
- Constrained Horn Clauses (CHCs) [Bjø+15]
  - used by SEAHORN [Gur+15]
  - checked by SPACER [KGC14] or Z3 [MB08]

PLCopen Safety Application



Typical Block Specification



Intuition for Logical Characterisation

- Reason about program semantics by leveraging Satisfiability Modulo Theories (SMT) solving

⇒ Characterise semantics via first order logic formulae

Condition Formula over the program's variables

$$[\![x > y + 1]\!] = x > y + 1$$

Statement Formula over pre- & post variables instances

$$[\![x := y + 1]\!] = \left(x' = y + 1\right) \land \left(y' = y\right)$$

Procedure Predicate over pre- & post variables instances

$$[\![\mathrm{abs}(x, x')]\!] = \left(x \geq 0 \to x' = x\right) \lor \left(x < 0 \to x' = -x\right)$$

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Unclear Characterisation of procedures with loops

Encoding the Running Example

Variables instances:

- $\vec{X} = (req, in, m, h.data, h.DiagCode, h.res, out)$
- $\vec{X}' = (req', in', m', h.data', h.DiagCode', h.res', out')$

Reachability facts & rules:

- Initial configuration reachable

$$init(\vec{X}) \to p_{Main}(0, \vec{X}, 0, \vec{X})$$

- Transitive reachability

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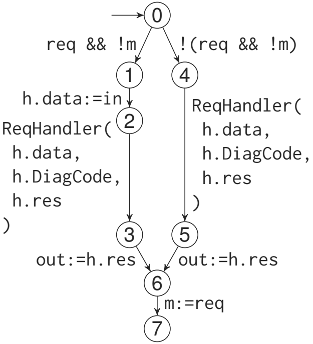

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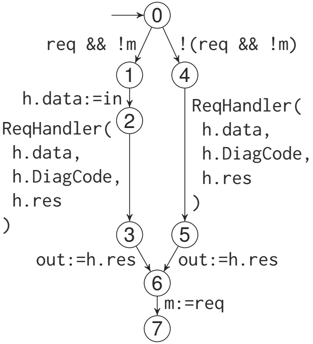

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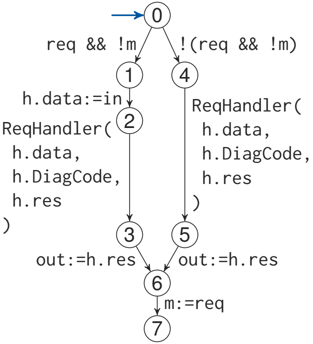

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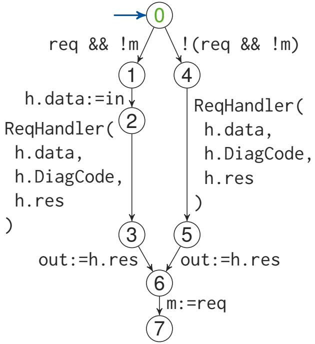

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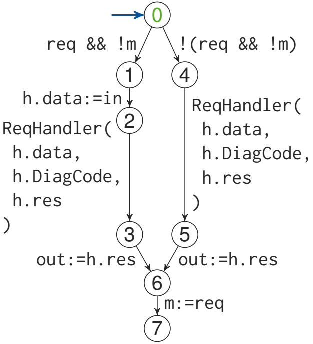

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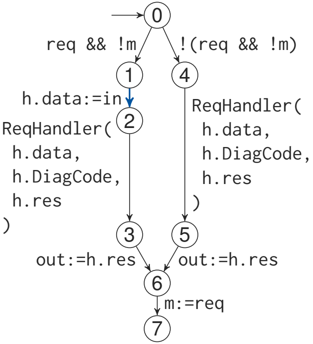

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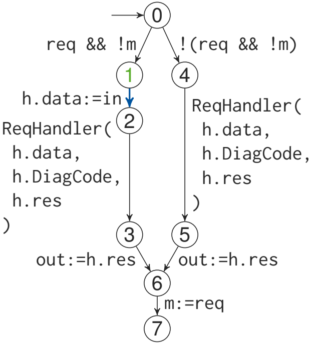

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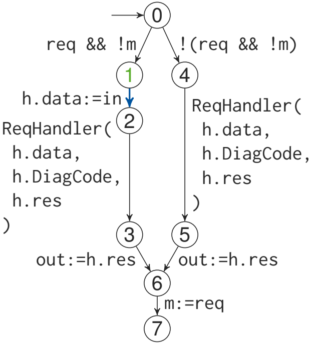

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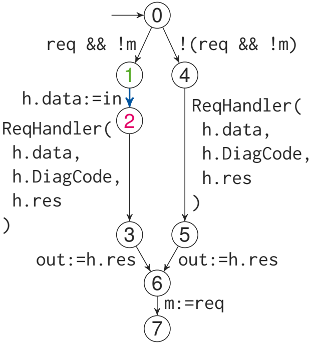

Encoding a Call

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- Transitive reachability ([illegible])

$$p_{Main}(l, \vec{X}, 2, \vec{X}')$$
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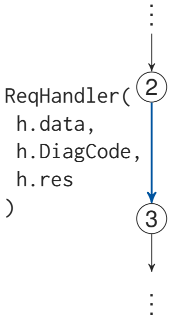
$$\rightarrow p_{Main}(l, \vec{X}, 3, \vec{X}'')$$



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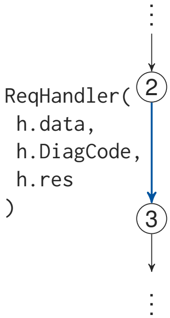

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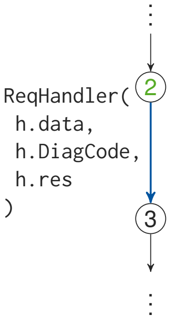

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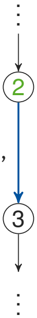

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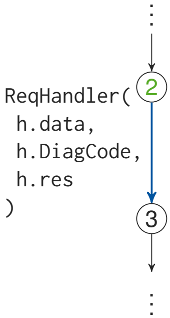

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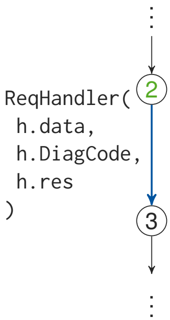

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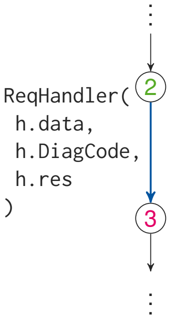

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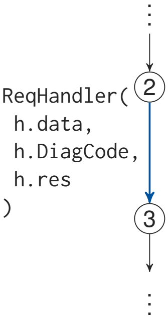

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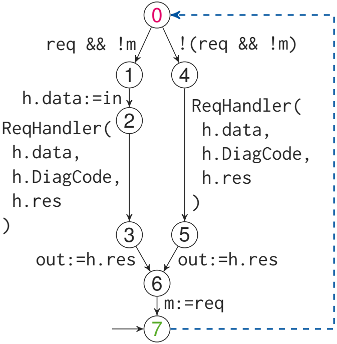
Implementation Details

- Possible cycle-edge encoding

$$p_{Main}(l, \vec{X}, 7, \vec{X}') \wedge id(\vec{X} \setminus \vec{X}_{in})$$

$$\rightarrow p_{Main}(l, \vec{X}, 0, \vec{X}'')$$

- Allow summaries for main block by modelling it like a call
- Reduce number of locations via Large Block Encoding



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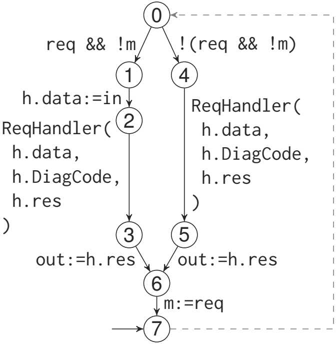
$$p_{Main}(l, \vec{X}, 7, \vec{X}') \wedge id(\vec{X} \setminus \vec{X}_{in})$$
$$\rightarrow p_{Main}(l, \vec{X}, 0, \vec{X}'')$$

- Allow summaries for main block by modelling it like a call
- Reduce number of locations via Large Block Encoding

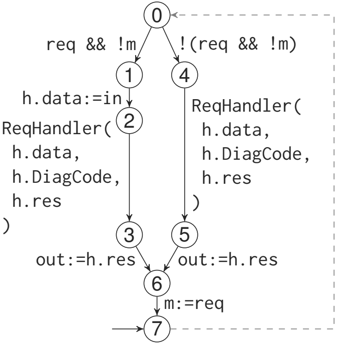


Implementation Details

- Possible cycle-edge encoding

$$p_{Main}(l, \vec{X}, 7, \vec{X}') \land id(\vec{X} \setminus \vec{X}_{in})$$
$$\rightarrow p_{Main}(l, \vec{X}, 0, \vec{X}'')$$

- Allow summaries for main block by modelling it like a call
- Reduce number of locations via Large Block Encoding



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