ARCADE.PLC

Symbolic Methods for Formal Verification of Industrial Control Software

Dimitri Bohlender, M. Sc. RWTH

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Informatik 11
Embedded Software
RWTH AACHEN UNIVERSITY

Outline

Introduction

- Formal Methods
- Setting
- Contributions & Related Work

CHC-based Safety Verification

Design and Verification of Restart-robust Software

Software-driven Systems

- ▶ Software drives the systems we rely on – hardware often off-the-shelf
- ▶ While many software bugs are not grave, some may be catastrophic:
  - Misinterpretation & no input validation led to radiation fatalities [Bor06]
  - Blackout after race condition affected 50 million people [Pow04]
- ▶ Writing “correct” software is hard – 50% of resources in testing [Mye12]

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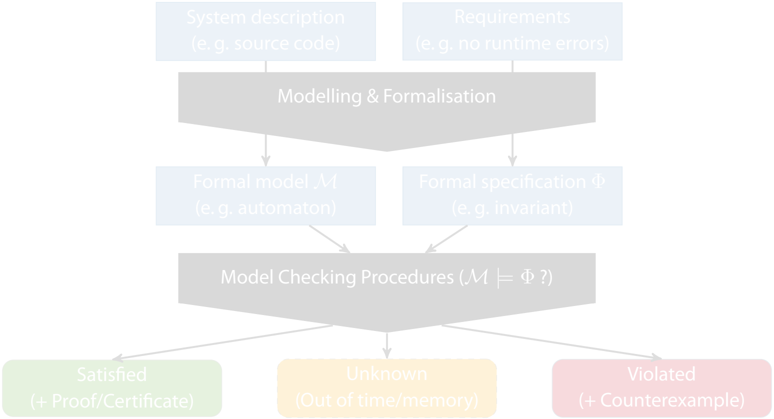
Formal Methods

- Based on mathematics, they enable rigorous modelling & reasoning
- Model checking (dis-)proves properties of interest



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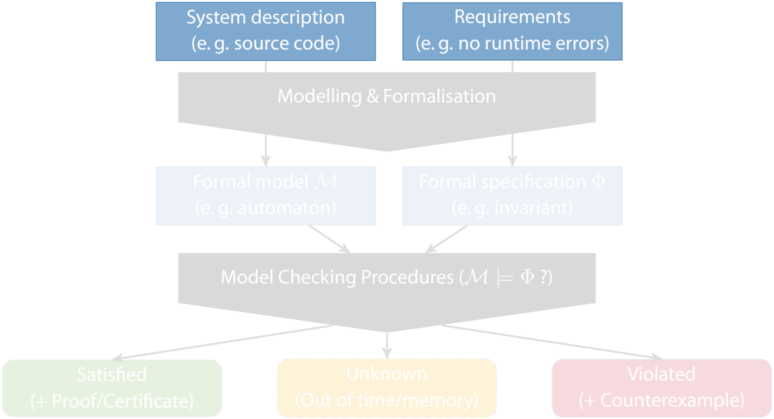

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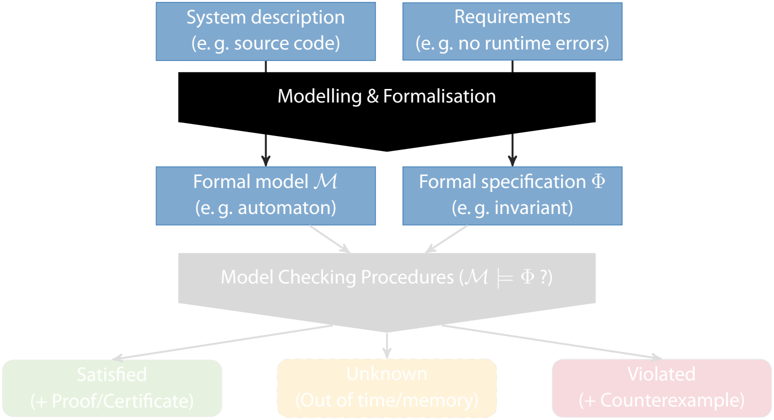

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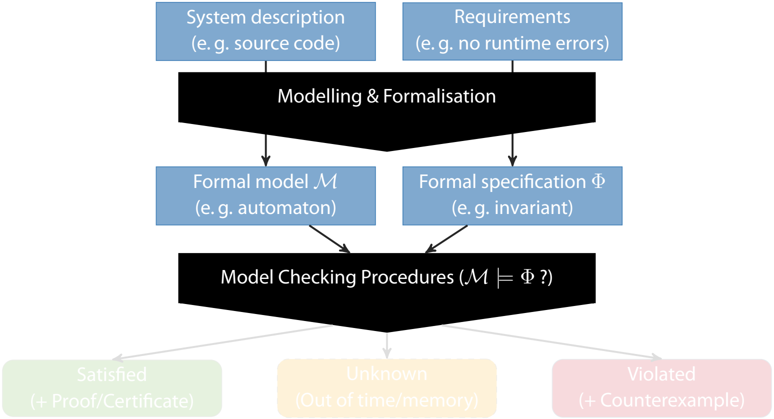

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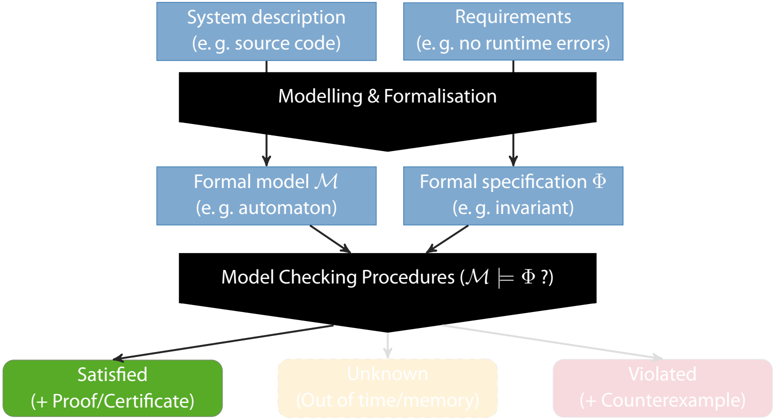

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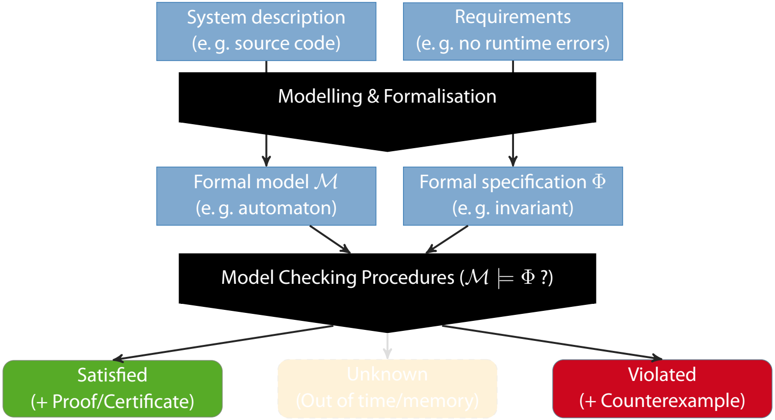

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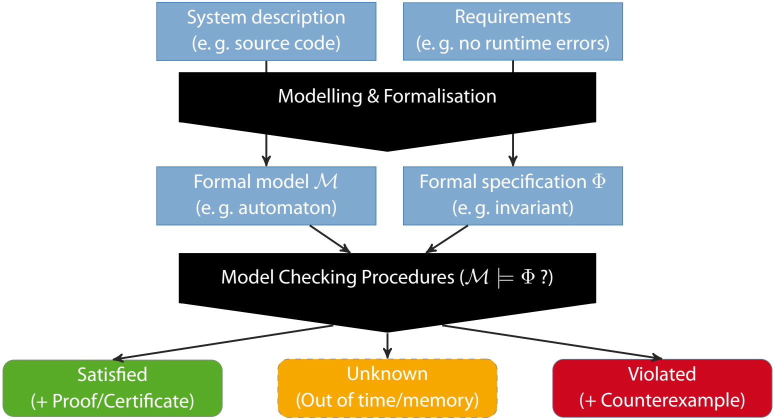
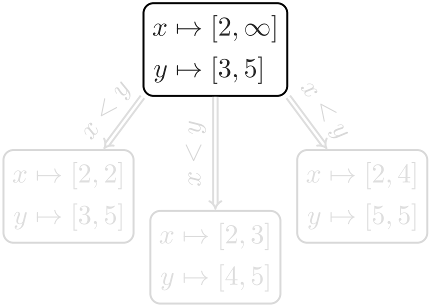


Explicit vs. Symbolic Methods



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\begin{aligned}
src(x, y) &:= 2 \leq x \\
&\quad \wedge 3 \leq y \leq 5 \\
T(x, y, x', y') &:= x < y \\
&\quad \wedge x' = x \wedge y' = y \\
bad(x', y') &:= x = 4
\end{aligned}
$$

- Explicit construction & search
- Precise representation needs space

- Implicit, lazy reasoning via SAT
- Exploits structure & symmetry

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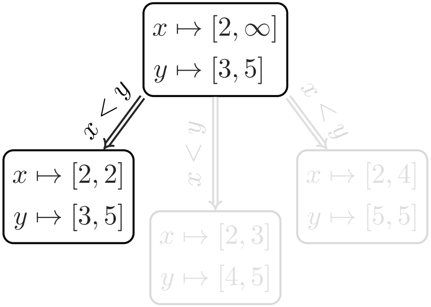

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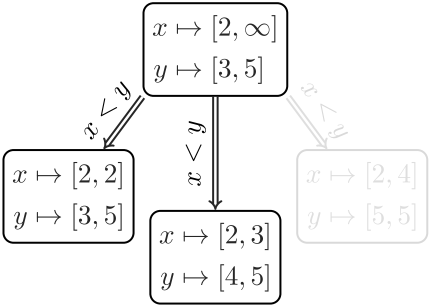

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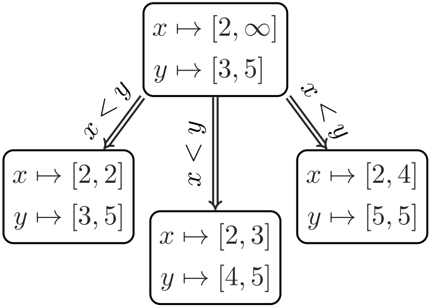
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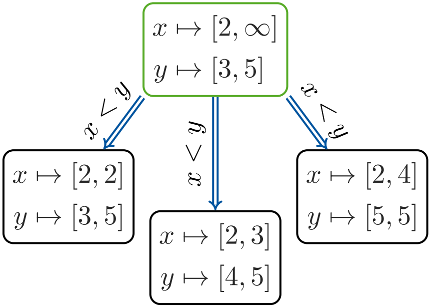

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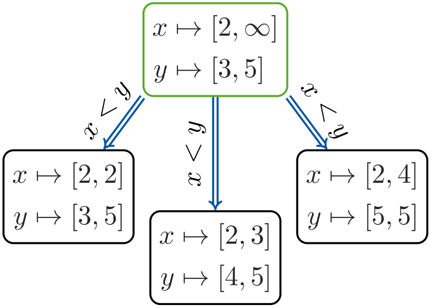

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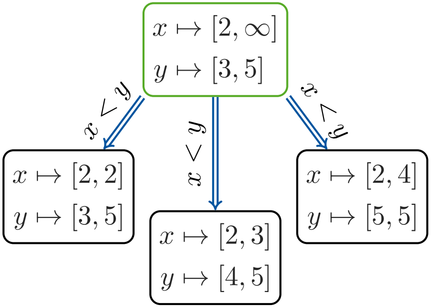

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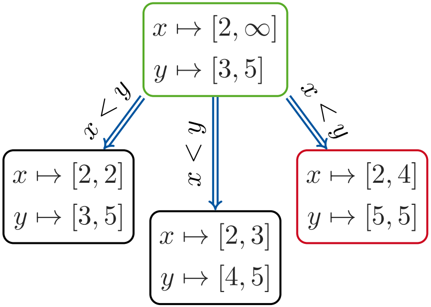

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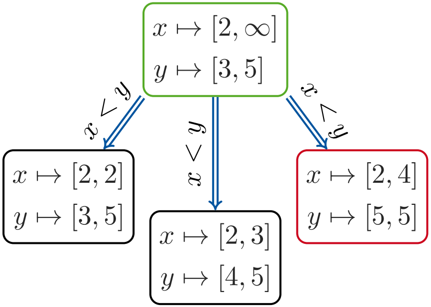

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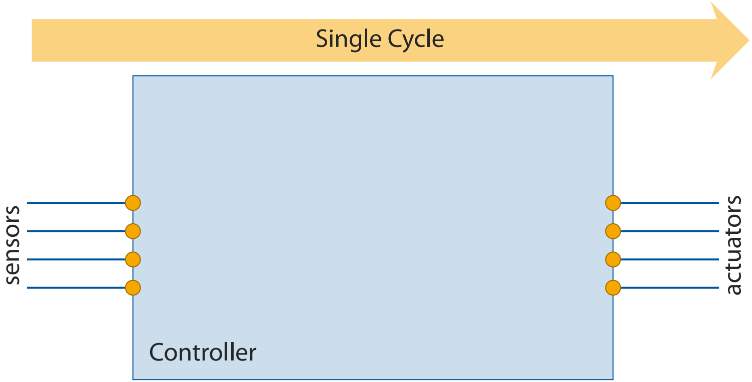
- Controllers realise reactive systems, repeatedly executing some task
- PLCs are rugged computers especially tailored to industrial control, e. g. for actuating assembly lines



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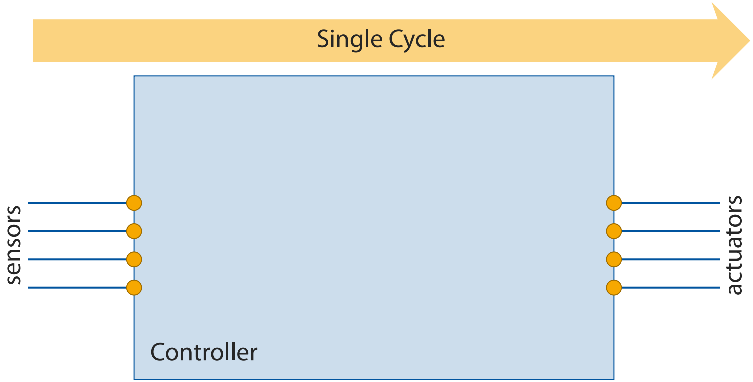

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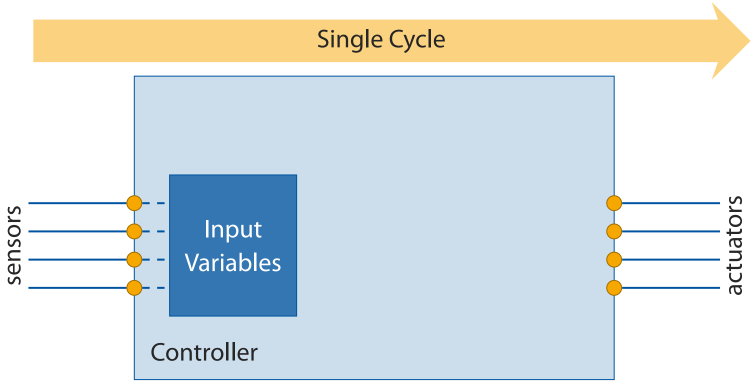

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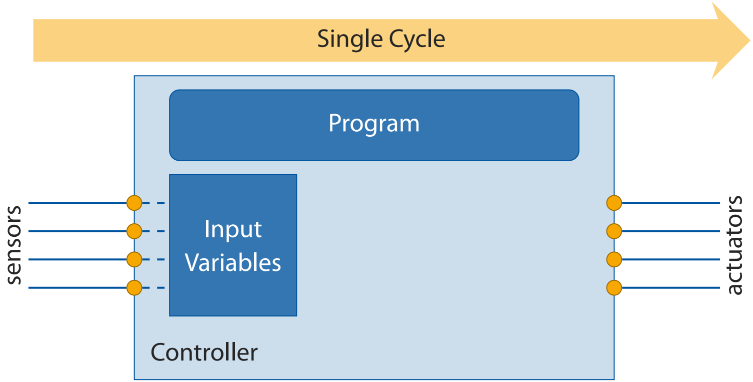

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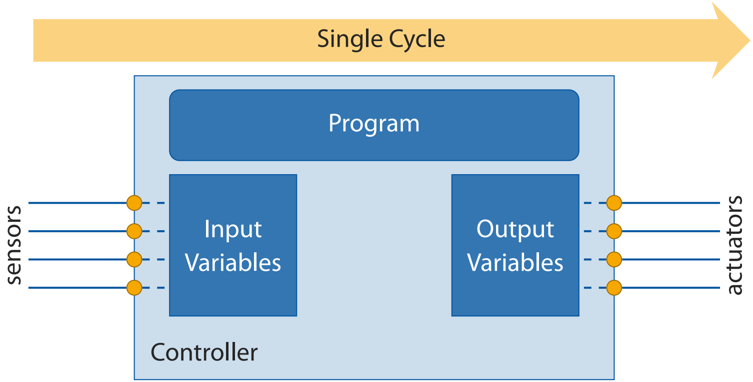

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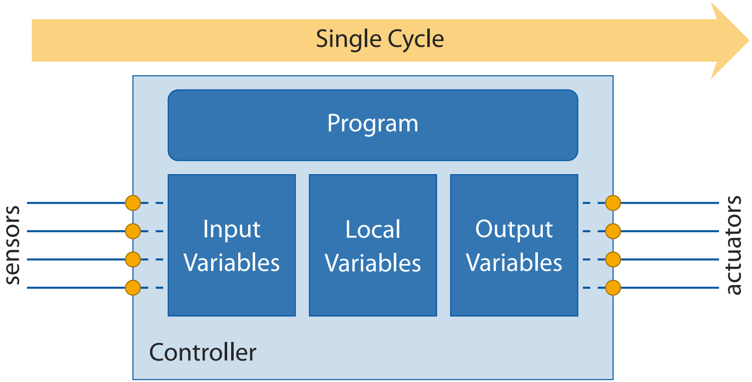

PLC Software

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PROGRAM R_TRIG
  VAR_INPUT
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  END_VAR
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    Q:BOOL;
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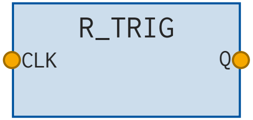

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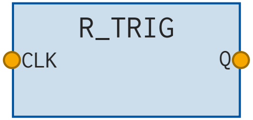

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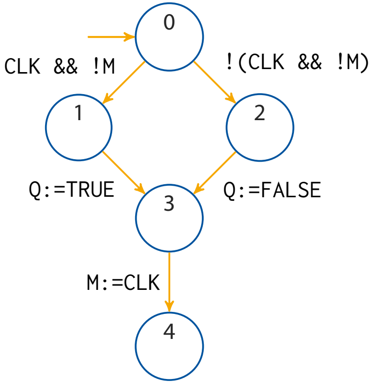

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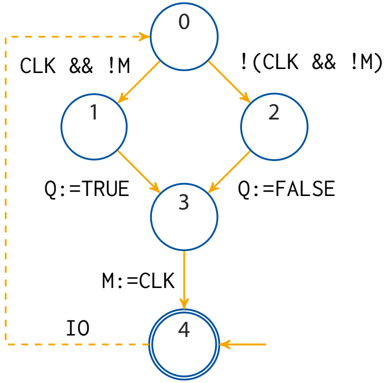

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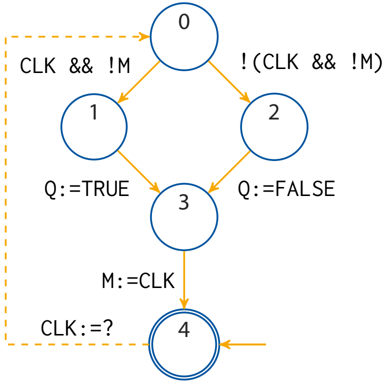
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Specifications

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⇒ Automation engineers and specifications always refer to the observable state

- Common specifications can be adapted to such cyle-step semantics, e. g.

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and checked with off-the-shelf backends

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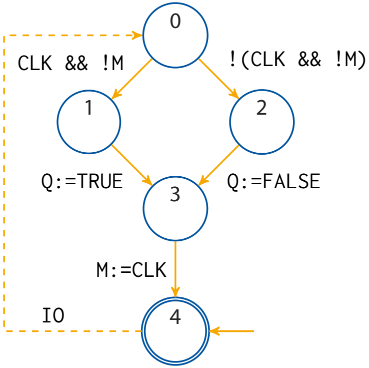

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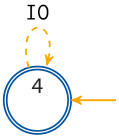

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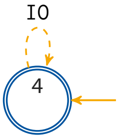

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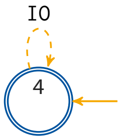

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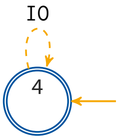

PLCopen

- An independent organisation "for efficiency in automation"
- Focus on technical specifications around IEC 61131-3, e. g.

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- Elementary modules implementing particular safety concepts
- User examples composed of those

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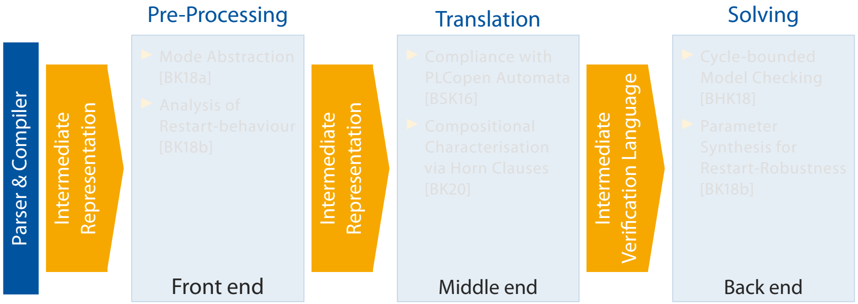
- Not included: Test generation [Boh+16], Explainability [Kö+19]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Analysis of Restart-behaviour [BK18b]
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Compositional Characterisation via Horn Clauses [BK20]
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Solving
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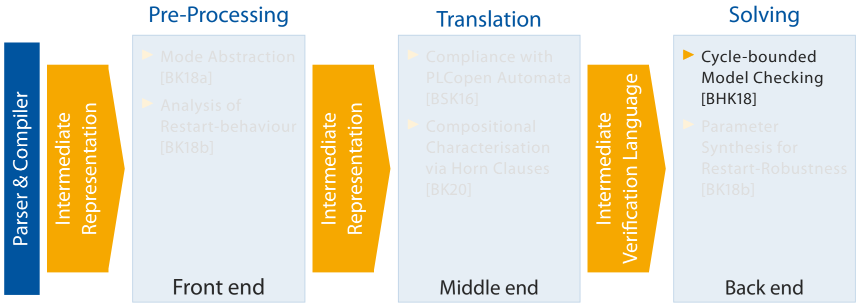
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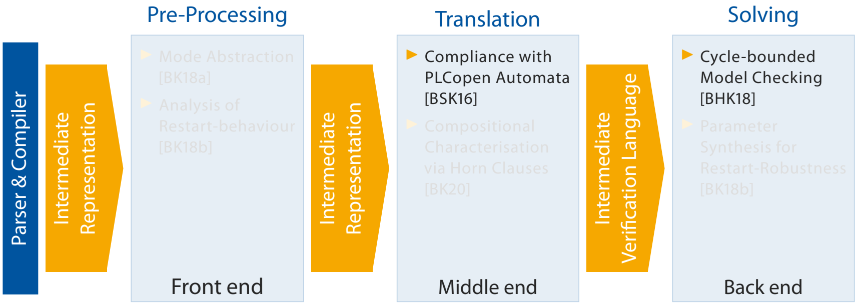
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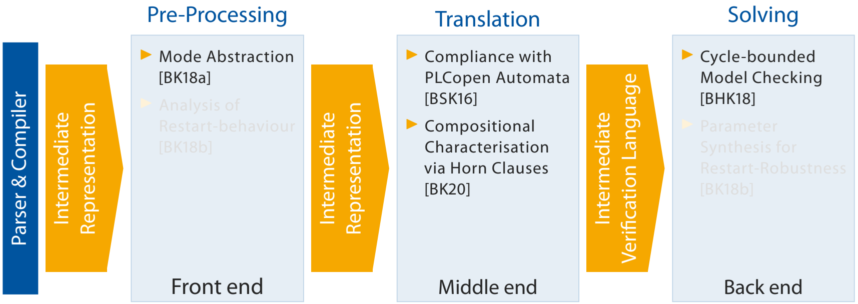
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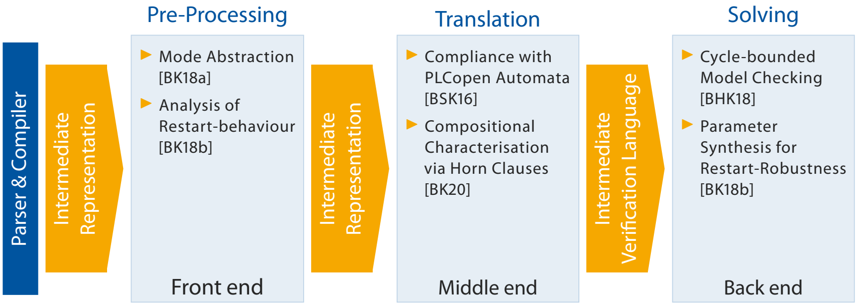
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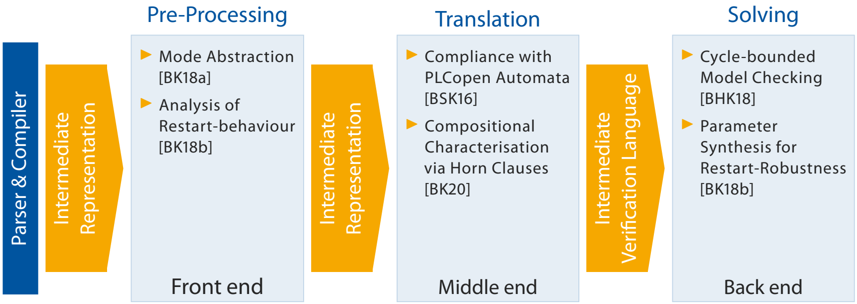
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Constrained Horn Clauses (CHCs)

- A reactive system is safe if an inductive invariant $Reach(\vec{X})$ exists, s. t. the following is SAT [MP95]:

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- Given sets of variables $\mathcal{V}$, function symbols $\mathcal{F}$, and predicates $\mathcal{P}$, a CHC is a formula

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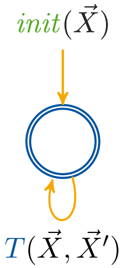

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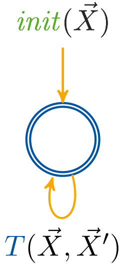

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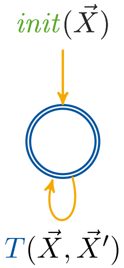

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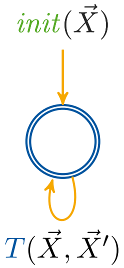

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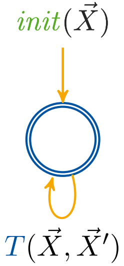

CHCs as Intermediate Verification Language

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  - Was competitive with highly tuned solvers – 3rd place at HWMCC'10

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⇒ Using CHC-solving, emerging tools were competitive at SV-COMP'15

Practical advantages:

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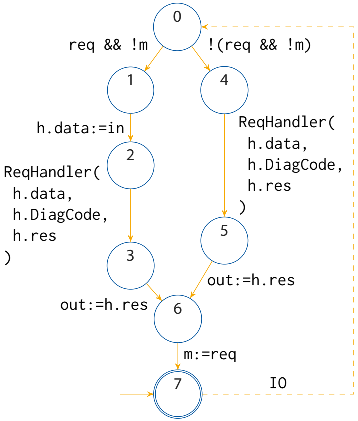
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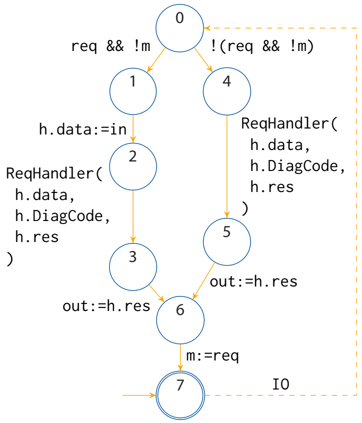
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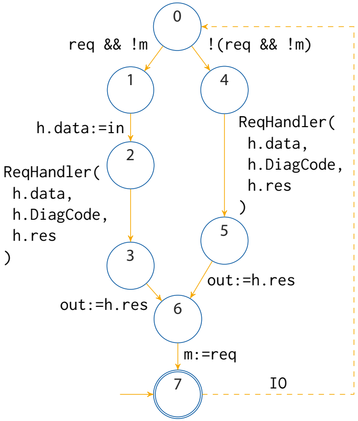
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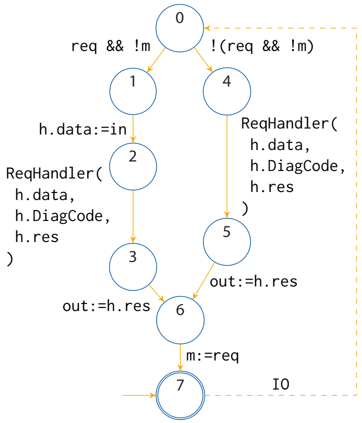
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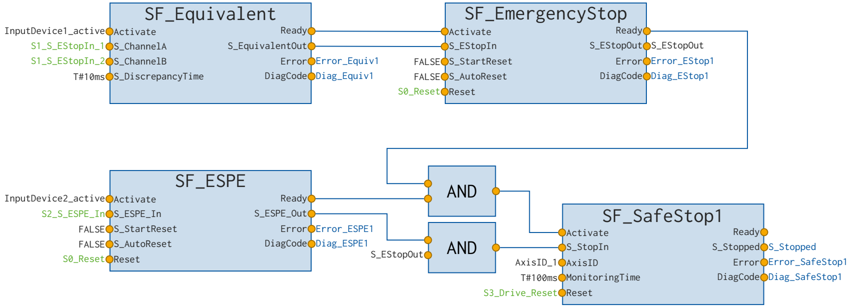
PLCopen Safety Application



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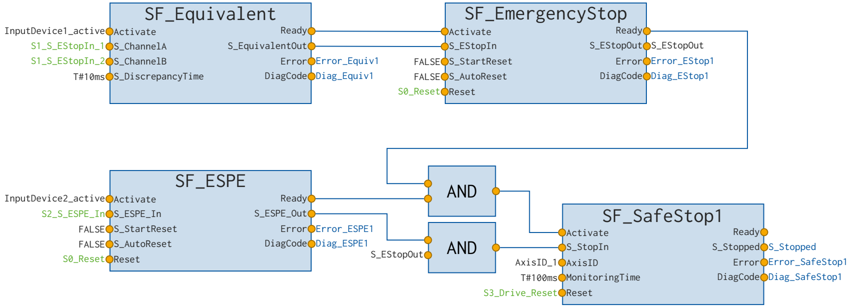

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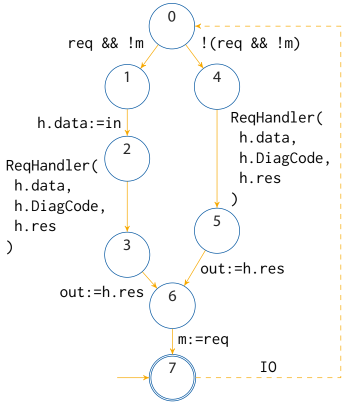
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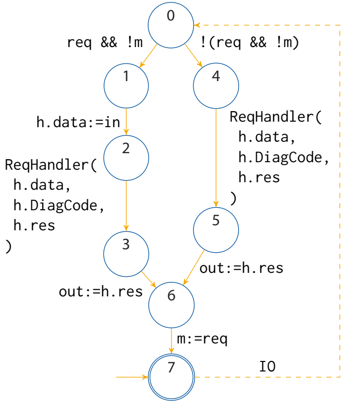
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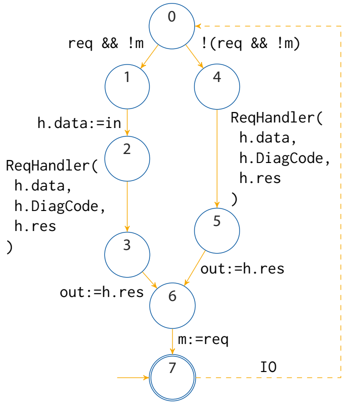
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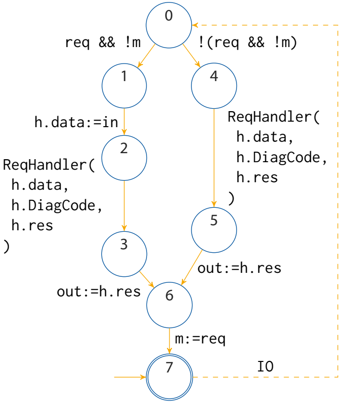
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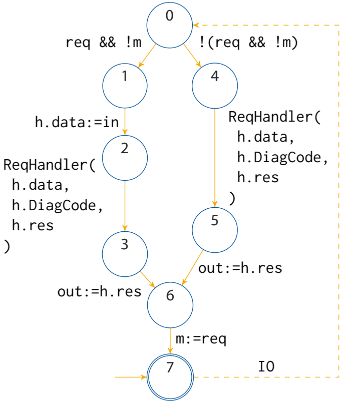
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1
4
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ReqHandler(h.data, h.DiagCode, h.res)
2
ReqHandler(h.data, h.DiagCode, h.res)
5
3
out:=h.res
out:=h.res
6
m:=req
7
IO

Compositional Characterisation

- Let P_i characterise a state $\vec{X}'$ at i, reachable from an entry state $\vec{X}$ of P:

$$Main_0(\vec{X}, \vec{X}') \wedge req' \wedge \neg m' \wedge \vec{X}'' = \vec{X}'$$
$$\rightarrow Main_1(\vec{X}, \vec{X}'')$$

- Gives a way to capture a block's I/O:

$$Main_7(\vec{X}, \vec{X}')$$

- Enables characterisation of calls, e. g.

$$Main_2(\vec{X}, \vec{X}') \wedge S(\vec{X}'_{ReqHandler}, \vec{X}''_{ReqHandler})$$
$$\wedge\ ReqHandler_{exit}(\vec{X}'_{ReqHandler}, \vec{X}''_{ReqHandler})$$
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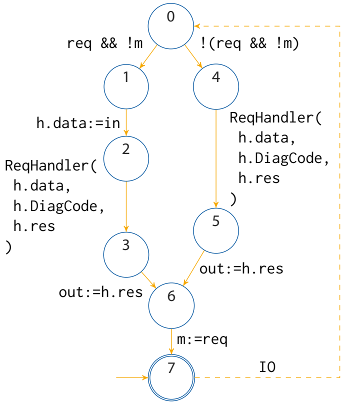
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Informatik 11 Embedded Software
RWTH AACHEN UNIVERSITY

Experiments

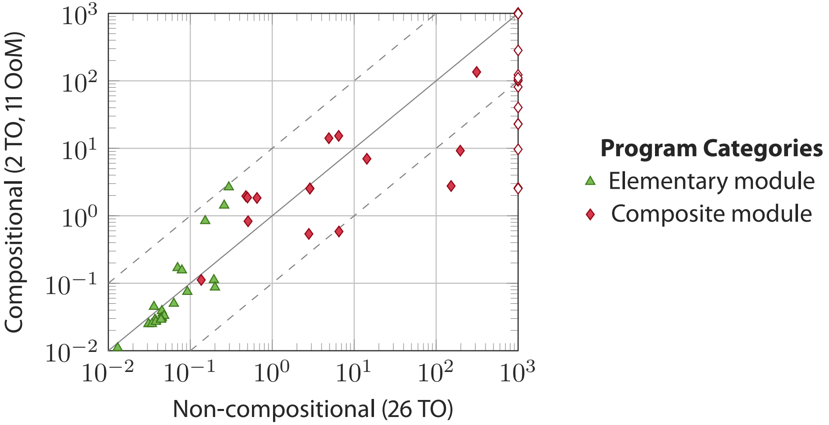
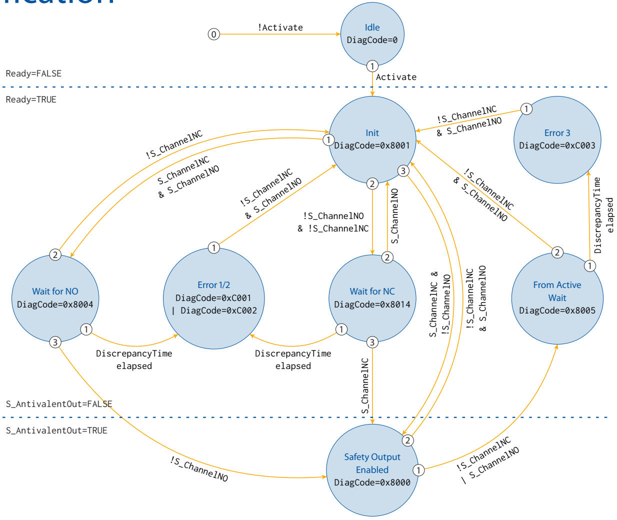


Figure: Time [s] spent on each verification task (n=64)

PLCopen Block Specification

- An engineer's mental model of a block often has state-machine semantics
- Such partitioning into different modes reduces the complexity
- May simplify reasoning for a verifier, too



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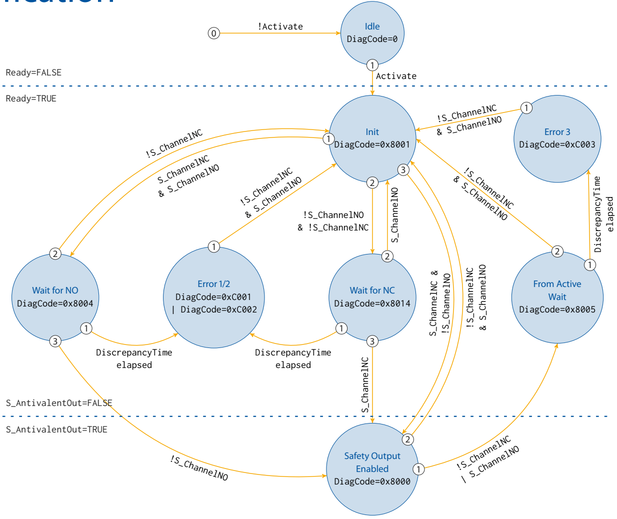

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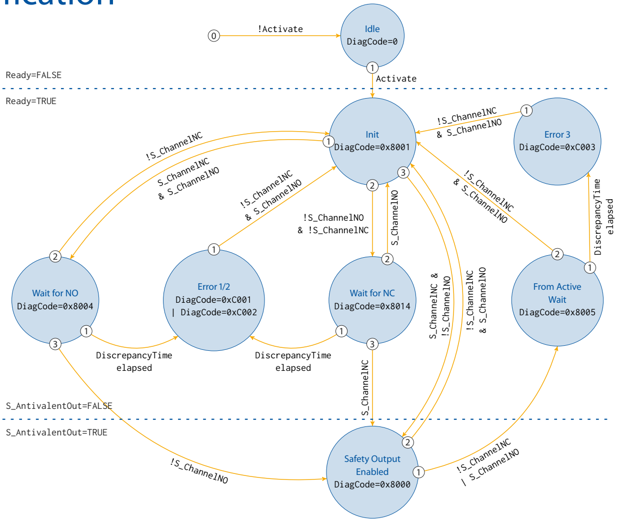
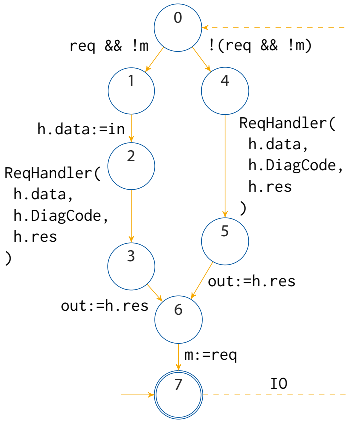


Mode Spaces in Model Checking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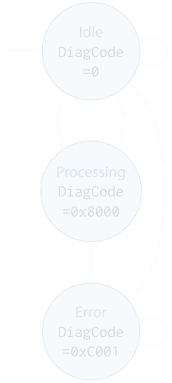

- Are requests processed in $\leq$ two execution cycles?

$\Rightarrow$ On a request, is the "Processing" mode reached in a single cycle?

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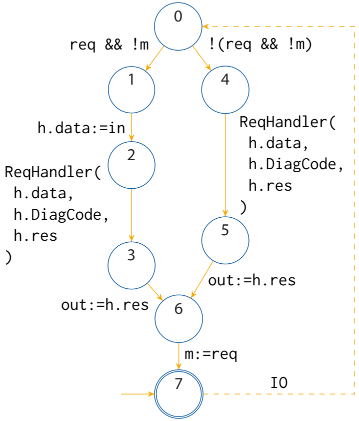

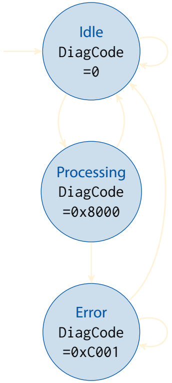

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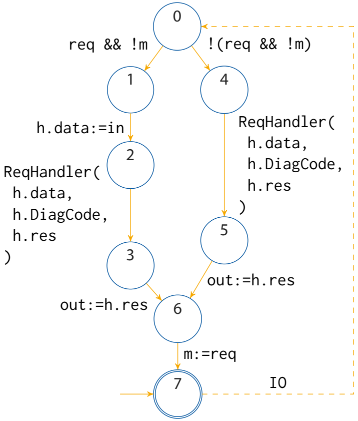
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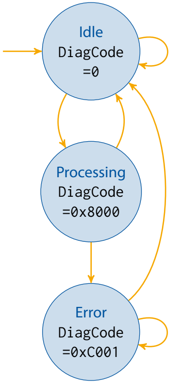

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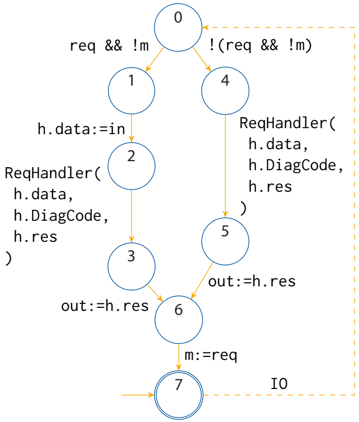

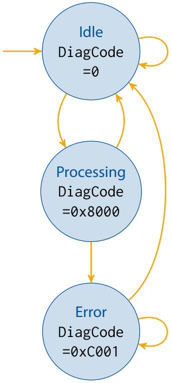

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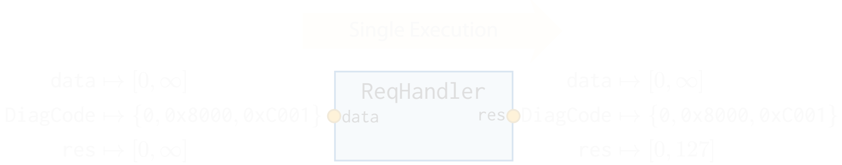
Mode Abstraction

Idea: Procedure's complexity needs to be low w.r.t. CHC-solving

$\Rightarrow$ Adapt value-set analysis (VSA)


Single Execution
data $\mapsto [0, \infty]$
DiagCode $\mapsto \{0, 0x8000, 0xC001\}$
res $\mapsto [0, \infty]$
ReqHandler
data
res
data $\mapsto [0, \infty]$
DiagCode $\mapsto \{0, 0x8000, 0xC001\}$
res $\mapsto [0, 127]$

1. Perform VSA on main CFA to approximate all variables' values
2. For each block type and mode, e. g. `ReqHandler` and `0x8000`
   2.1 Keep VSA's values but fix source mode
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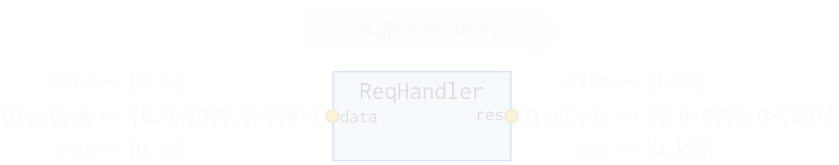

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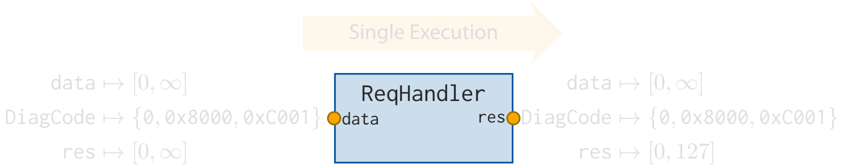

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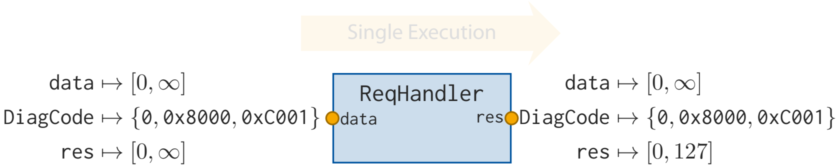
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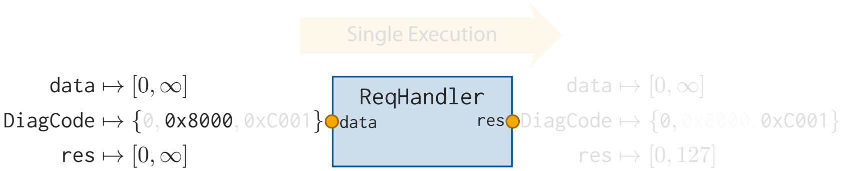

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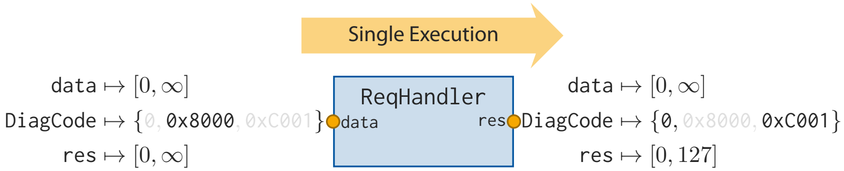

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Mode Space as Call Summary

- Mode space constrains possible transitions

⇒ Yields call summary $S_{ReqHandler}(\vec{X}_h, \vec{X}'_h)$:

$$
\begin{aligned}
&(h.DiagCode = \texttt{0} \rightarrow h.DiagCode' = \texttt{0} \\
&\qquad \vee\ h.DiagCode' = \texttt{0x8000}) \\
\wedge\ &(h.DiagCode = \texttt{0x8000} \rightarrow h.DiagCode' = \texttt{0} \\
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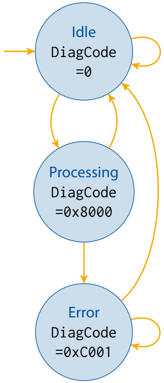
\end{aligned}
$$



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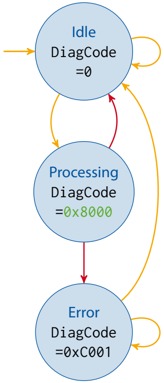

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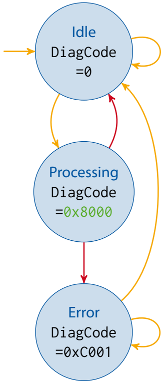

Experiments

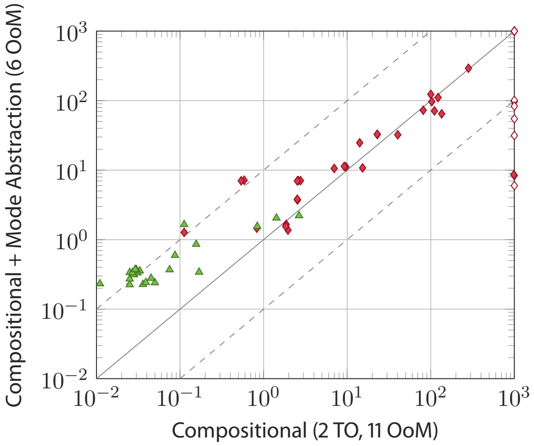

Figure: Time [s] spent on mode abstraction and solving CHCs ($n = 64$)

Restart-Behaviour

However:

- A proof holds w.r.t. the formal model – not the real system

⇒ Model is usually missing behaviour enabled by hardware

Battery-backed memory & restart-functionality:

- Non-volatile state variables allow for "restart-robust" designs
- Restarts may be triggered by a watchdog timer, power surge, …
- Writing to battery-backed memory immediate or delayed to cycle end

⇒ Choice of retain-variables and reasoning left to developer

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Toy Example: Invariant $a \geq 0$

- Initially $fs \mapsto true, a \mapsto 0, b \mapsto 0$
- Nominal behaviour compliant?

In context of restarts

- Let the flag `fs` be retained
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- Fixable for delayed writes?
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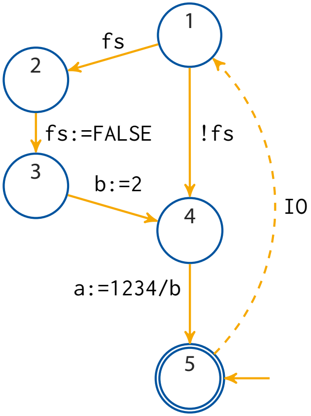

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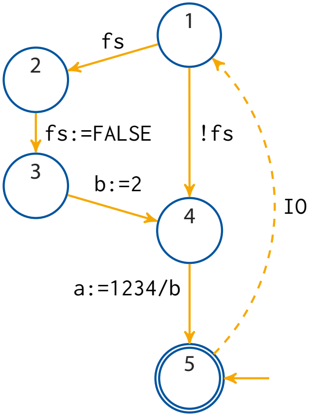

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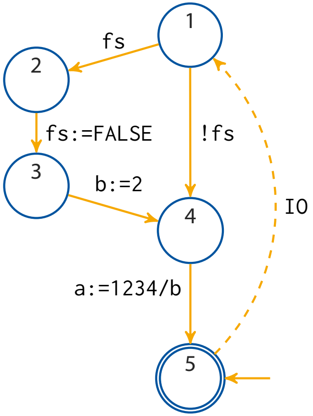

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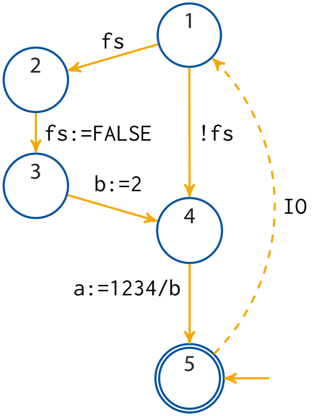

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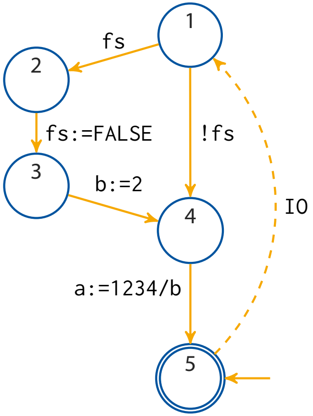

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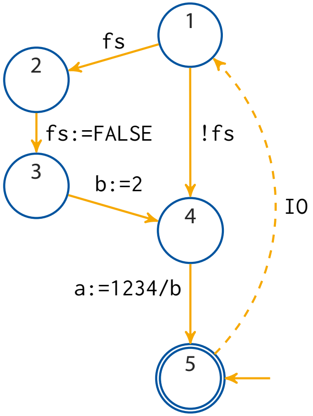

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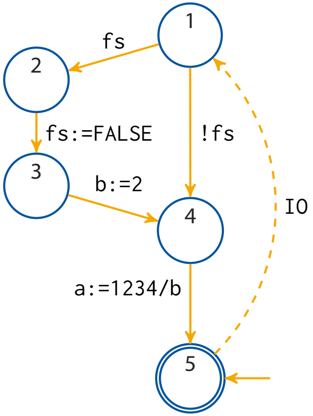

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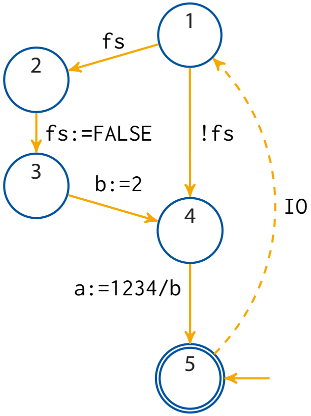

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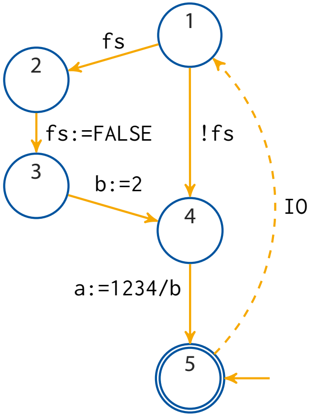

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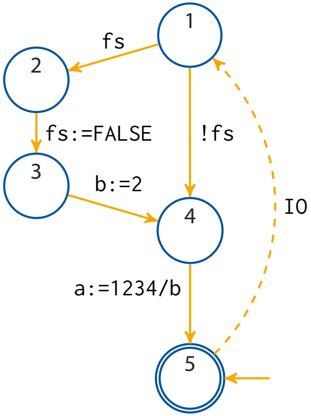

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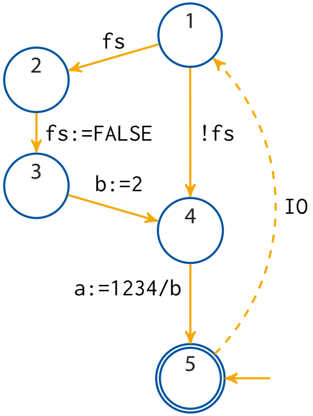

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- Initially $fs \mapsto true, a \mapsto 0, b \mapsto 0$
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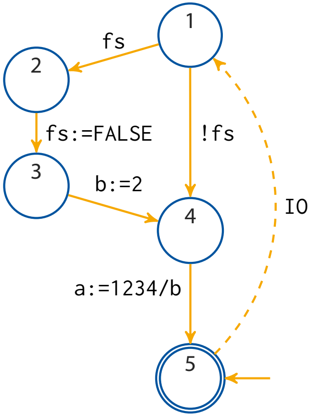

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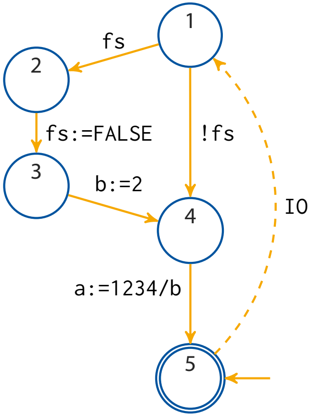
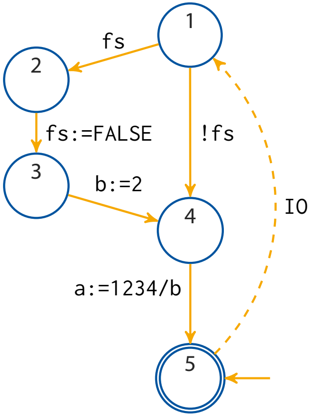


Delayed Write Semantics

- Approached by instrumenting the CFA with restart-behaviour
- Observation: On restart, operations since last cycle are irrelevant

⇒ Model as nondeterministic choice: restart in next cycle?

- Handle immediate writes similarly



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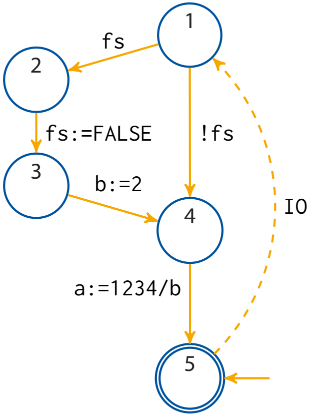

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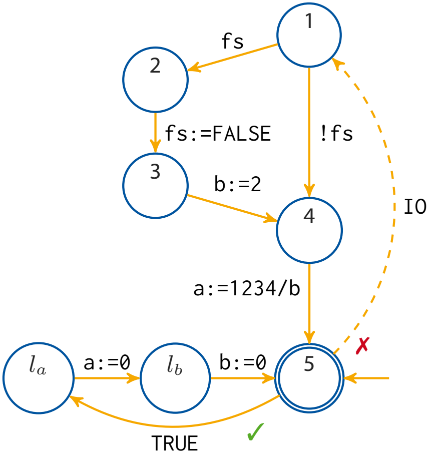

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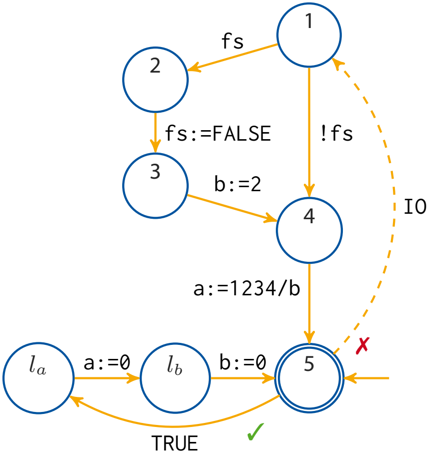

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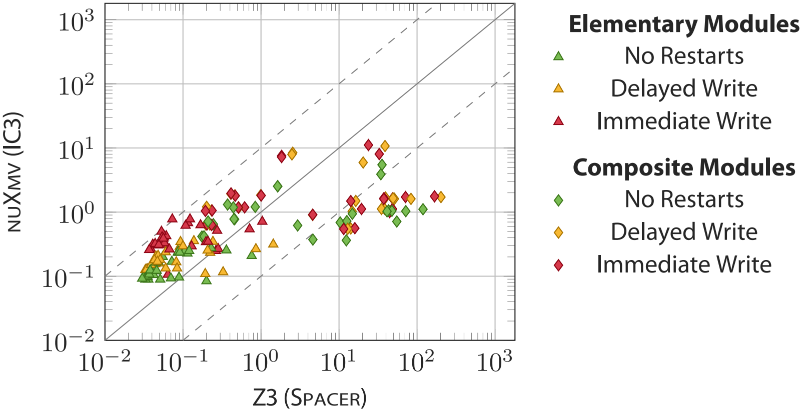


Figure: Time [s] spent checking restart-robustness w.r.t. each spec ($n = 3 \cdot 56$)

CHC-based Parameter Synthesis

- No aid in picking safe configuration of retain variables

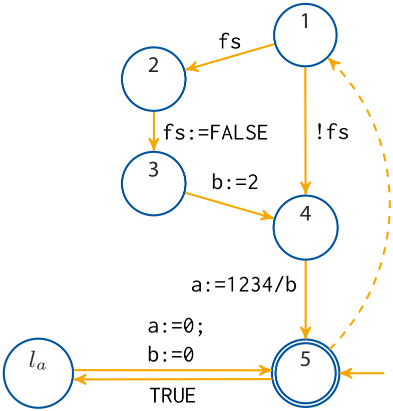
⇒ Add Boolean parameter `ret_v` for each non-retain variable v

- Derived CHCs check whether all configurations are robust

$$\forall \vec{V} \underbrace{\ldots}_{\text{body}} \rightarrow h(\vec{V})$$

- Parameter synthesis is

$$\exists \vec{V}_{par} \forall \vec{V} \setminus \vec{V}_{par} \cdots \rightarrow h(\vec{V})$$



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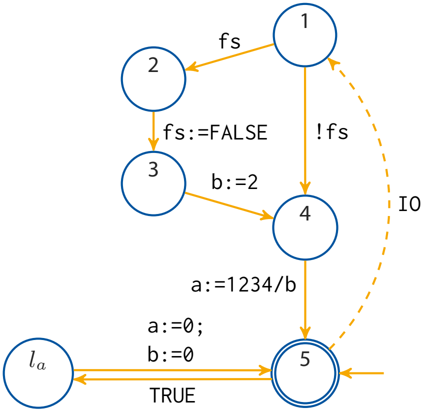

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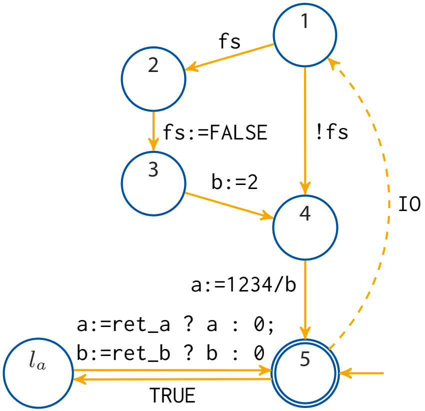

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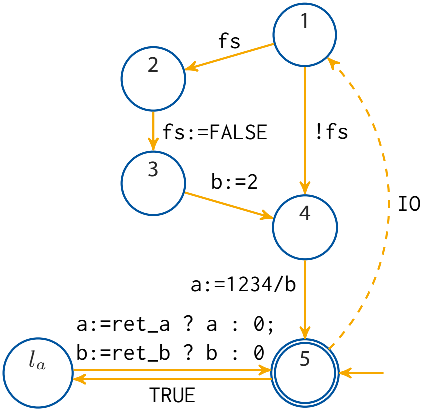

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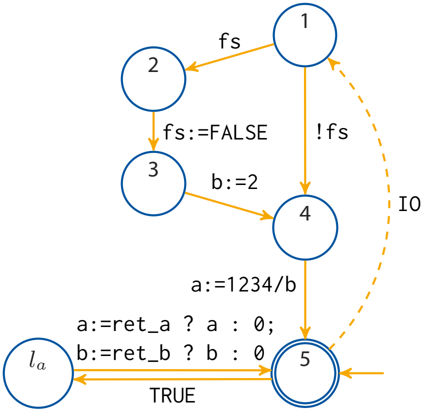

Counterexample-Guided Parameter Synthesis

$$\exists \vec{V}_{par} \forall \vec{V} \setminus \vec{V}_{par} \; \cdots \rightarrow h(\vec{V})$$

Observations:

- $\exists\forall$-quantified Horn clauses harder than regular CHCs (48 TO)
- Our special case: existential quantification over Booleans

Idea:

- Manage choice and reuse efficient check for fixed parameters
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Example

- Make the program restart-robust w.r.t. $a \geq 0$ under delayed writes
- Let `fs` be required to be retained

Process:

1. Start with $safe(\vec{V}_{par}) = true$
2. Backend finds counterexample
   $$c = \neg ret_a \wedge \neg ret_b$$
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   $$c_g = \neg ret_b$$
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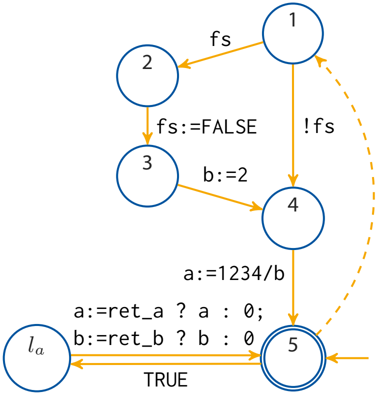

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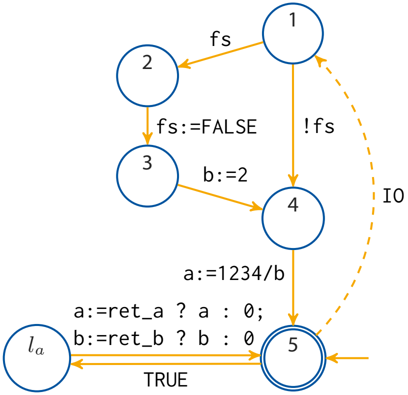

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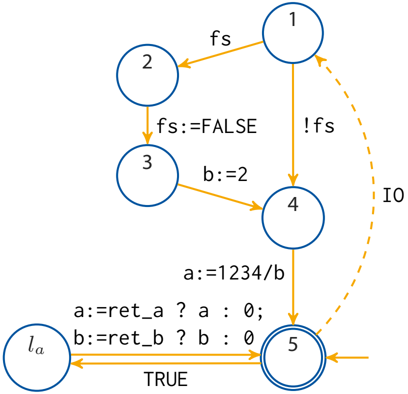

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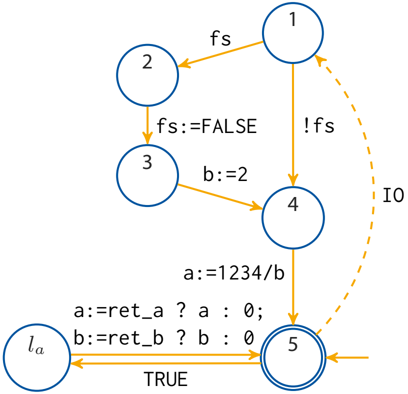

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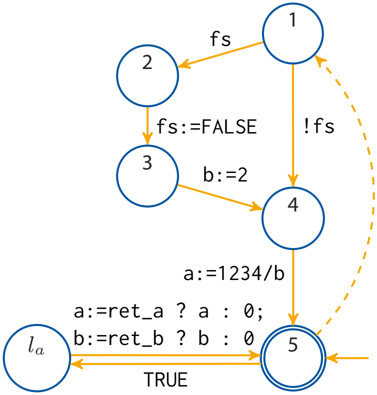

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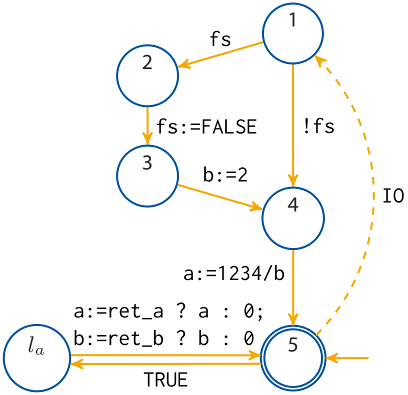

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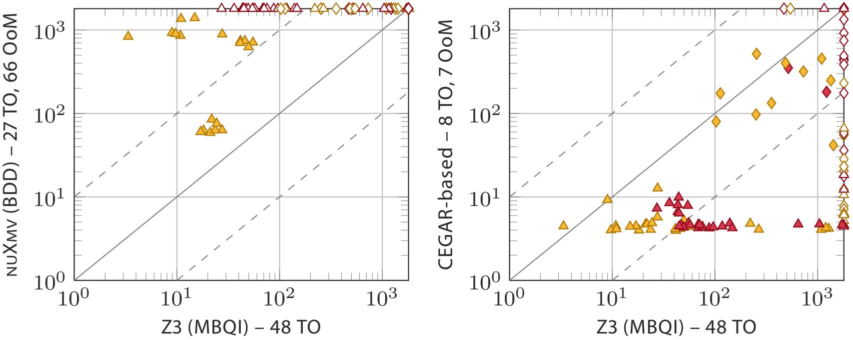

Figure: Time [s] spent on synthesis of restart-robust configurations ($n = 2 \cdot 56$)

Summary

- Software verification machinery hardly used in industrial control
- Most focus on checking common specifications with existing tooling

- We proposed SMT-based verification procedures
- Competitive with existing tooling
- Enabled verification of previously
  - “problematic” tasks
  - unsupported domain-specific specifications

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